

library ieee;

use ieee.std\_logic\_1164.all;

entity test2andbus is

port (

a: in std\_logic\_vector(7 downto 0);

b: in std\_logic\_vector(7 downto 0);

c: out std\_logic\_vector(7 downto 0)

);

end test2andbus ;

architecture BEHAVIOR of test2andbus is

begin

c(0)<= a(0) and b(1);

c(1)<= a(1) and b(0);

c(7 downto 2)<=a(7 downto 2) and b(7downto 2);

end BEHAVIOR;